REMARKS

Claims 9-39 are pending, with claims 9, 18, 19, 28 and 33 being independent. Claims 1-8 have been canceled. Claims 28 and 33 have been amended.

In response to the rejection under 35 U.S.C. §112, second paragraph, claims 28 and 33 have been amended to more clearly recite that etching the "first conductive film" results in a laminate structure that includes "a first conductive layer." The "first conductive layer" is different from the recited "second conductive layer."

With respect to the double patenting rejection, applicants will consider whether to file a terminal disclaimer in the event that the claims of the '282 and '334 applications are allowed prior to this application. However, applicants note that the Examiner appears to make impermissible use of the specifications of the '282 and '334 applications in making the rejections.

Accordingly, applicants submit that all claims are in condition for allowance.

Attached is a marked-up version of the changes being made by the current amendment.

Applicants ask that all claims be allowed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

Version with markings to show changes made

In the claims:

Claims 1-8 have been cancelled.

Claim 28 and 33 have been amended as follows:

28. (Amended) A method of manufacturing a semiconductor device comprising steps of:

forming a semiconductor layer on an insulating surface;

forming an insulating film on said semiconductor layer;

laminating a first conductive film and a second conductive film on said insulating film;

forming a second conductive layer with a first width;

adding an impurity element to said semiconductor layer using said second conductive layer with said first width as a mask to form a high concentration impurity region;

etching said first conductive film to form a first electrode comprising a laminate structure of **[said]** a first conductive layer with a second width and said second conductive layer with a third width;

etching said second conductive layer to form a second electrode comprising a laminate structure of said first conductive layer with said second width and said second conductive layer with a fourth width;

adding said impurity element to said semiconductor layer through said first conductive layer using said second conductive layer with said fourth width as a mask to form a low concentration impurity region; and

etching said first conductive layer to form a third electrode comprising a laminate structure of said first conductive layer with a fifth width and said second conductive layer with said fourth width.

33. (Amended) A method of manufacturing a semiconductor device comprising steps of:

forming a semiconductor layer on an insulating surface;

forming an insulating film on said semiconductor layer;

laminating a first conductive film and a second conductive film on said insulating film;

forming a second conductive layer with a first width;

adding an impurity element to said semiconductor layer using said second conductive layer with said first width as a mask to form a high concentration impurity region;

etching said second conductive layer to form said second conductive layer with a second width;

adding an impurity element to said semiconductor layer through said first conductive film using said second conductive layer with said second width as a mask to form a low concentration impurity region; and

etching said first conductive film to form an electrode comprising a laminate structure of **[said]** a first conductive layer with a third width and said second conductive layer with said second width.